Customer No.: 31561
Application No.: 10/064,395
Docket No.: 8219-US-PA

In The Claims

Please amend claims as follows:

[c1]

1. (currently amended) A programmable memory controller, comprising:

a main memory controller for sending a request signal when ~~thesaid~~ said programmable memory controller ~~needs to accessed~~ accesses data from a memory unit;

a command decoder for decoding ~~thesaid~~ said request signal to produce a plurality of command signals;

a ~~cycleperiod~~ period setting device for decoding a control signal to produce a ~~cycleperiod~~ period setting signal, wherein ~~thesaid~~ said control signal controls [~~the~~] a maintenance period of ~~thesaid~~ said command signal;

a command-sequencing device for ordering and outputting ~~thesaid~~ said command signals according to the command signals and ~~thesaid~~ said~~cycleperiod~~ period setting signals; and

a command signal output device for receiving ~~thesaid~~ said ordered command signals and ~~thesaid~~ said~~cycleperiod~~ period setting signals, and controlling ~~thesaid~~ said output of ordered command signals outputted to the memory during ~~thesaid~~ said maintenance period, according to indications provided by ~~thesaid~~ said~~cycleperiod~~ period setting signals.

[c2]

2. (currently amended) The memory controller of claim 1, wherein ~~thesaid~~ said memory is a synchronous dynamic random access memory (SDRAM).

[c3]

3. (currently amended) The memory controller of claim 1, wherein ~~thesaid~~ said memory is a double data rate dynamic random access memory (DDR DRAM).

[c4]

4. (currently amended) The memory controller of claim 1, wherein ~~thesaid~~ said maintenance period is set according to the travel distance of ~~thesaid~~ said command signal.

[c5]

5. (currently amended) The memory controller of claim 4, wherein ~~thesaid~~ said travel distance includes trace length between ~~thesaid~~ said control chipset of ~~thesaid~~ said memory controller and ~~thesaid~~ said memory slot pin of ~~thesaid~~ said memory.

[c6]

6. (currently amended) The memory controller of claim 4, wherein ~~thesaid~~ said maintenance period can be a first period or a second period, ~~such that the~~wherein the first period ~~command signal is up for~~represents as one clock cycle, ~~if the command signal has a first period~~ and the second period ~~command signal is up for two cycles if the command signal has a second period~~represents as two clock cycles.

[c7]

7. (currently amended) The memory controller of claim 6, wherein ~~thesaid~~ said maintenance period is the first period if ~~thesaid~~ said travel distance is lower than a pre-defined distance and the second period and ~~thesaid~~ said maintenance period is the second period if ~~thesaid~~ said travel distance exceeds ~~thesaid~~ said pre-defined distance.

[c8]

8. (currently amended) The memory controller of claim 7, wherein ~~thesaid~~ said pre-defined distance is about 2500 mils.

[c9]

9. (currently amended) A memory access structure having a programmable memory controller therein, wherein ~~thesaid~~ said memory access structure controls a plurality of command signals for accessing data inside a memory unit, comprising:

a control chipset having a built-in programmable memory controller, wherein ~~thesaid~~ said control chipset controls ~~thesaid~~ a maintenance period of ~~thesaid~~ said command signals output from ~~thesaid~~ said programmable memory controller when ~~thesaid~~ said control chipset needs to access data inside ~~thesaid~~ said memory unit; and

a memory slot for receiving ~~thesaid~~ said command signals and transferring ~~thesaid~~ said command signals to the memory unit, wherein ~~thesaid~~ said maintenance period of ~~thesaid~~ said

command signals is determined according to the control signals~~, and thesaid maintenance period is set according to the distance between thesaid memory controller and thesaid memory slot~~.

[c10]

10. (currently amended) The memory access structure of claim 9, wherein ~~thesaid~~ said programmable memory controller further comprises:

a main memory controller for sending out a request signal when ~~thesaid~~ said control chipset needs to access data within ~~thesaid~~ said memory unit;

a command decoder for decoding ~~thesaid~~ said request signal and reading out ~~thesaid~~ said command signals;

a ~~cycleperiod~~ period setting device for producing a ~~cycleperiod~~ period setting signal according to the control signal, wherein ~~thesaid~~ said control signal controls the maintenance period of ~~thesaid~~ said command signal;

a command-sequencing device for ordering and producing new command signals according to incoming command signals and ~~thesaid~~ said~~cycleperiod~~ period setting signals; and

a command signal output device for controlling ~~thesaid~~ said maintenance period of ~~thesaid~~ said ordered command signals going outputted to the memory slot according to indications provided by ~~thesaid~~ said~~cycleperiod~~ period setting signals.

[c11]

11. (currently amended) The memory access structure of claim 9, wherein ~~thesaid~~ said memory is a synchronous dynamic random access memory (SDRAM).

[c12]

12. (currently amended) The memory access structure of claim 9, wherein ~~thesaid~~ said memory is a double data rate dynamic random access memory (DDR DRAM).

[c13]

13. (canceled)

[c14]

14. (currently amended) The memory access structure of claim 13, wherein ~~thesaid~~ said travel distance includes trace length between ~~thesaid~~ said control chipset and ~~thesaid~~ said memory slot pin position.

[c15]

15. (currently amended) The memory access structure of claim 14, wherein ~~thesaid~~ said maintenance period can be a first period or a second period such that ~~thesaid~~ said command signal is up for one ~~cycleperiod~~ period if ~~thesaid~~ said command signal has a first period and ~~thesaid~~ said command signal is up for two cycles if ~~thesaid~~ said command signal has a second period.

[c16]

16. (cancelled)

[c17]

17. (currently amended) The memory access structure of claim 15, wherein ~~thesaid~~ said maintenance period is the first period if ~~thesaid~~ said travel distance is lower than a pre-defined distance and the second period and ~~thesaid~~ said maintenance period is the second period if ~~thesaid~~ said travel distance exceeds the pre-defined distance.

[c18]

18. (currently amended) The memory access structure of claim ~~16~~ 17, wherein ~~thesaid~~ said pre-defined distance is about 2500 mils.

[c19]

19. (currently amended) A motherboard having a memory unit and a memory controller thereon such that maintenance period for command signals traveling from~~thesaid~~ said memory controller to the memory unit is determined by their distance of separation, ~~thesaid~~ said motherboard comprising:

a memory slot for receiving command signals and sending ~~thesaid~~ said command signals to the memory plugged into ~~thesaid~~ said memory slot, wherein ~~thesaid~~ said maintenance period of ~~thesaid~~ said command signal is set according to a control signal, and ~~thesaid~~ said maintenance period is related to the distance of separation between ~~thesaid~~ said memory controller and ~~thesaid~~ said memory slot;

a memory controller, comprising:

a main memory controller for sending a request signal when ~~thesaid~~ said programmable memory controller needs to access data from a memory unit;

a command decoder for decoding ~~thesaid~~ said request signal to produce a plurality of command signals;

a ~~cycleperiod~~ period setting device for decoding a control signal to produce a ~~cycleperiod~~ period setting signal, wherein ~~thesaid~~ said control signal controls ~~thesaid~~ said maintenance period of ~~thesaid~~ said command signal;

a command-sequencing device for ordering and outputting ~~thesaid~~ said command signals according to the command signals and ~~thesaid~~ said~~cycleperiod~~ period setting signals; and

a command signal output device for receiving~~thesaid~~ said ordered command signals and ~~thesaid~~ said~~cycleperiod~~ period setting signals, and controlling ~~thesaid~~ said ordered command signal outputted ~~of ordered command signal~~ to the memory during ~~thesaid~~ said maintenance period according to indications provided by ~~thesaid~~ said~~cycleperiod~~ period setting signal.

[c20]

20. (currently amended) The motherboard of claim 19, wherein ~~thesaid~~ said memory is a synchronous dynamic random access memory (SDRAM).

[c21]

21. (currently amended) The motherboard of claim 19, wherein ~~thesaid~~ said memory is a double data rate dynamic random access memory (DDR DRAM).

[c22]

22. (cancelled)

[c23]

23. (currently amended) The motherboard of claim ~~22~~ 19, wherein ~~thesaid~~ said travel distance includes trace length between ~~thesaid~~ said control chipset of ~~thesaid~~ said memory controller and ~~thesaid~~ said memory slot pin position.

[c24]

24. (currently amended) The motherboard of claim ~~22~~ 19, wherein ~~thesaid~~ said maintenance period can be a first period or a second period, wherein ~~such that~~ the first period represents as ~~command signal is up for~~ one clock cycle ~~if the command signal has a first period~~, and the second period ~~command signal is up for~~ represents as two cycles ~~if the command signal has a second periodrepresents as two clock cycle~~.

[c25]

25. (currently amended) The motherboard of claim 24, wherein ~~thesaid~~ said maintenance period is the first period if ~~thesaid~~ said travel distance is lower than a pre-defined distance and the

second period and ~~thesaid~~ said maintenance period is the second period if ~~thesaid~~ said travel distance exceeds ~~thesaid~~ said pre-defined distance.

[c26]

26. (currently amended) The motherboard of claim 25, wherein ~~thesaid~~ said pre-defined distance is about 2500 mils.

[c27]

27. (currently amended) A method of controlling [~~the~~] a maintenance period of command signals according to travel distance between a memory unit and a memory controller, comprising the steps of:

generating a request signal when data inside ~~thesaid~~ said memory unit needs to be accessed;

decoding ~~thesaid~~ said request signal to produce a plurality of command signals, wherein ~~thesaid~~ said commands signals are sent to the memory unit to initiate data accessing operations;

decoding a control signal to produce a ~~cycleperiod~~ period setting signal, wherein ~~thesaid~~ said control signal controls ~~thesaid~~ said maintenance period of ~~thesaid~~ said command signal;

sequencing and outputting ~~thesaid~~ said sequenced command signals according to ~~thesaid~~ said input command signals and ~~thesaid~~ said~~cycleperiod~~ period setting signals; and

controlling ~~thesaid~~ said sequenced command signal outputted~~going~~ to the memory unit within ~~thesaid~~ said maintenance period according to indications provided by ~~thesaid~~ said~~cycleperiod~~ period setting signals.

[c28]

28. (currently amended) The method of claim 27, wherein ~~thesaid~~ said memory is a synchronous dynamic random access memory (SDRAM).

[c29]

29. (currently amended) The method of claim 27, wherein ~~thesaid~~ said memory is a double data rate dynamic random access memory (DDR DRAM).

[c30]

30. (cancelled)

[c31]

31. (currently amended) The method of claim ~~30~~ 27, wherein ~~thesaid~~ said travel distance includes trace length between ~~thesaid~~ said control chipset of ~~thesaid~~ said memory controller and ~~thesaid~~ said memory slot pin position.

[c32]

32. (currently amended) The method of claim ~~30~~ 27, wherein ~~thesaid~~ said maintenance period can be a first period or a second period, wherein ~~such that~~ the first period ~~command signal is up for~~ represents as one clock cycle, ~~if the command signal has a first period~~ and the second period ~~the command~~ represents as ~~signal is up for~~ two clock cycles ~~if the command signal has a second period~~, ~~and~~wherein the first period is shorter than the second period.

[c33]

33. (currently amended) The method of claim 32, wherein ~~thesaid~~ said maintenance period is the first period if ~~thesaid~~ said travel distance is lower than a pre-defined distance and the second period and ~~thesaid~~ said maintenance period is the second period if ~~thesaid~~ said travel distance exceeds ~~thesaid~~ said pre-defined distance.

[c34]

34. (currently amended) The method of claim 33 ~~31~~, wherein ~~thesaid~~ said pre-defined distance is about 2500 mils.